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EXAMINER	
MALSAWMA, LALRINFAMKIM HMAR	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 12/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/812,480	PADHI ET AL.
	Examiner	Art Unit
	Lex Malsawma	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-21 and 23-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-21 and 23-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/11/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. Some of the references listed on form PTO-1449 (filed on August 11, 2005) have been lined through because the publication dates for these references were not provided.

Claim Objections

2. Claim 20 is objected to because of the following informalities:

"conductive material" should read "conductive element", since claim 1 recites "conductive element".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1, 2, 4, 5, 7-17 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Havas et al. (4,090,006; hereinafter "**Havas**") in view of **Jones** (4,339,305).

Regarding claim 1:

Havas discloses (in Figs. 1E-1H) a method of processing a semiconductor substrate, comprising the steps of:

depositing a protective layer 24/26 on a topographically substantially flat substrate surface comprising an exposed conductive element 8 (Fig. 1E-1F);

selectively removing a portion of the protective layer 24/26 to expose the conductive element 8 of the substrate surface (Fig. 1F);

depositing a metallic passivating layer 28/34' (Fig. 1G) onto the exposed conductive element, wherein stray metallic passivating material is also deposited on the protective layer (i.e., the passivating material deposited on top of the protective layer 24/26 is considered to be "stay material" because it will be removed/discarded by a following process step); and

removing at least a portion of the protective layer 24/26 from the substrate after deposition of the metallic passivating layer, wherein the stray metallic passivating material deposited on the protective layer is also removed (Fig. 1H).

Havas is silent with respect to a particular process used for depositing the metallic passivation layer, i.e., Havas **lacks** specifically utilizing electroless deposition. However, since

Havas is silent with respect to the deposition process, one of ordinary skill in the art would have utilize any suitable process known in the art for depositing the metallic passivating layer.

Jones is **cited to show** it was very well known in the art that an electroless deposition process is well suited for depositing a metallic passivating layer 24 (Fig. 4 and Col. 4, lines 52). Furthermore, note that Jones shows that any stray metallic passivating material is removed when the protective layer 14 is removed using a "lift-off" process (see Figs. 4-5), i.e., the "passivating and lift-off process" shown by Jones is similar to the process disclosed by Havas, accordingly Jones shows that an electroless deposition process is well suited for Havas' process.

Because Havas does not specify any particular deposition process, which can or cannot be utilized, it would have been obvious to one of ordinary skill in the art to use an electroless deposition because Jones shows that electroless deposition is well suited for forming a metallic passivating layer similar to that in Havas' disclosure.

Regarding claims 2, 4, 5, 7-11, 14-16 and 20:

Havas discloses the substrate surface comprises dielectric material 20 (Fig. 1E) in which the conductive element 8 is disposed;

a portion of the thickness (as well as the entire thickness) of the protective layer is removed (Figs. 1G-1H);

the step of depositing a protective layer 24/26 is accomplished by spin on deposition (note Col. 3, lines 60-62 and Col. 6, lines 29-32, wherein the process for forming protective layer 24-26 is the same as that for forming layer 4/6);

the protective layer 24/26 comprises an organic material (e.g., photoresist 24, note that photoresist is also a dielectric material), wherein the steps for depositing and processing the photoresist protective layer comprise the steps of:

depositing a photoresist layer 24 over the substrate surface; and

exposing and developing the photoresist under conditions that do not degrade the substrate surface to expose a selected region of an underlying layer 8 (Fig. 1F);

wherein the exposed and developed photoresist is removed after deposition of the metallic passivation layer by wet chemical etch (Col. 5, lines 18-28); and

wherein the conductive component comprises copper (Col. 4, lines 35-36).

Regarding claims 12 and 13:

These claims depend from claim 9 and contain limitations associated with an amorphous carbon protective layer; however, claim 9 only requires that the organic material for the protective layer be either photoresist or amorphous carbon. Therefore, regardless of the additional limitations associated with an amorphous carbon layer, Havas (in view of Farrar) renders these claims obvious because Havas discloses the organic material is photoresist.

Regarding claims 17 and 19:

Havas discloses steps for depositing and processing the protective layer 24/26 comprise the steps of:

depositing an intermediate layer 24 on the substrate surface (Fig. 1F);

depositing a protective layer 26 on the intermediate layer 24 (Fig. 1F);

selectively removing the protective layer to expose the intermediate layer; and

selectively removing the intermediate layer under conditions that do not degrade the conductive element 8 (Fig. 1F), wherein the intermediate layer 24 comprises a dielectric material (i.e., a photoresist). Note that both layers "24" and "26' are selectively removed at least with respect to the conductive element 8.

Regarding claim 21:

Havas discloses the passivating layer can be a material including an alloy of tantalum (note Col. 4, lines 53-55 and Col. 6, lines 42-44).

6. Claims 3 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Havas** (in view of **Jones**) as applied to claims 1 and 17 above, and further in view of **Farrar** (6,426,289 B1).

Regarding claim 3:

Havas (in view of Jones) **lacks** the substrate surface comprises a low-k dielectric material; however, note that Havas discloses the substrate surface comprises an insulator/dielectric material 20 (Fig. 1E and Col. 5, lines 44-45). Farrar **teaches** low-k material such as polyimide is well suited for a dielectric layer 7 (Fig. 6 and Col. 3, lines 25-35), which serves as a substrate surface, where polyimide is just one of a variety of dielectric materials suitable for layer "7". Note that Farrar discloses dielectric materials such as silicon oxide (i.e., glass) and silicon nitride are also well known to be suitable for use on a substrate surface. It would have been obvious to one of ordinary skill in the art to modify Havas (in view of Jones) by specifically utilizing a low-k dielectric material for layer "20" because Farrar teaches that low-k dielectric materials are just one of a plurality of well-known materials suitable for an

insulating layer formed on a substrate surface. Note that it has been held to be within the general skill of a worker in the art to select a known material (e.g., polyimide) on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Regarding claim 18:

Farrar discloses utilizing multi-layers that are selectively etchable in order to achieve a simplified, CVD-less method of forming a barrier layer (for a metal layer), which prevents metal contamination in an IC (note Col. 2, lines 28-42). Farrar discloses the multi-layers include an intermediate layer 17 (Fig. 8), and a protective layer 21, wherein the intermediate layer 17 functions as an etch-stop layer when the protective layer 21 is removed (note process flow in Figs. 9-10). It would have been obvious to one of ordinary skill in the art to modify Havas (in view of Jones) by incorporating multi-layers comprising an intermediate etch-stop layer and a photoresist protective layer (as taught by Farrar) because the multi-layers would allow a simplified, CVD-less method for forming a barrier layer that prevents metal contamination.

7. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Havas** (in view of **Jones)** as applied to claim 1 above, and further in view of Amelio et al. (4,639,380; hereinafter "**Amelio**").

Regarding claim 23:

Havas (in view of Jones) discloses electrolessly depositing a metallic passivating layer by depositing an initiation layer, followed by depositing a metallic passivating layer on the initiation layer by electroless plating (Note Jones, Col. 4, lines 27-43). Havas (in view of Jones) **lacks**

specifically disclosing a cleaning step after depositing the initiation layer. Amelio is **cited to show** it was well known in the art to include a cleaning step prior to depositing a metallic layer (i.e., a metal plating) in an electroless plating process. Amelio discloses that a typical electroless plating process includes forming a seed/initiation layer (Col. 1, lines 39-40); cleaning the substrate after forming the initiation layer (Col. 1, lines 58-61); and depositing a metallic passivating layer. It would have been obvious to one of ordinary skill in the art to modify Havas (in view of Farrar) by performing a cleaning step after depositing the initiation/seed layer because Amelio shows/teaches that an electroless plating process typically incorporates such a cleaning step in order to ensure the quality of the metal coating (note Amelio, Col. 1, lines 59-61).

8. Claim 24, 26, 28-31, 33 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Farrar** (6,426,289 B1) in view of Lopatin et al. (6,479,902 B1; hereinafter "**Lopatin**").

Regarding claims 24, 26, 28 and 29:

Farrar discloses a method of processing a semiconductor substrate, comprising the steps of:

depositing a protective layer (comprising "17" and "21", note Figs. 7-8 and Col. 4, lines 64-67) on a topographically substantially flat substrate surface comprising a conductive element 1 (copper, Col. 3, lines 20-21);

steps for processing the protective layer to expose the conductive element (Fig. 8);

steps for depositing a metallic passivating layer 23 (Fig. 9 and Col. 5, lines 1-2) onto the conductive element and depositing stray metallic passivating material 23 on the protective layer

(note the "stray" passivating material 23 directly on top of layer "21" in Fig. 9, i.e., the passivating material 23 on top of layer "21" will be removed when layer "21" is removed, therefore, the passivating material on top of layer "21" is "stray material", since it is not needed for the electroless deposition of conductor 13 in a subsequent step, note Fig. 11 and Col. 5, lines 21-32);

steps for removing at least a portion of the protective layer from the substrate after the deposition (Figs. 9-10 and Col. 5, lines 21-22);

where steps for depositing and processing the protective layer comprise the steps of:

steps for depositing an intermediate layer 17 (Figs. 7-8) on the substrate surface;

steps for depositing a protective layer 21 on the intermediate layer;

steps for exposing and developing the protective layer 21 to expose the intermediate layer (Fig. 8 and Col. 4, lines 63-67);

steps for etching the intermediate layer 17 under conditions that do not degrade the conductive element; and

wherein the steps for depositing and processing a photoresist/dielectric (21/17) protective layer comprise the steps of:

steps for depositing the photoresist/dielectric layer over the substrate surface;

steps for exposing and developing the photoresist 21 under conditions that do not degrade the conductive element (Col. 4, lines 63-65); and

steps for etching the dielectric protective layer 17 under conditions that do not degrade the conductive elements (i.e., the photoresist layer 21 and the intermediate/dielectric protective layer 17 are formed of a material significantly different from the material for the

conductive element 1; therefore, the etching process for removing the photoresist and/or the intermediate/dielectric protective layer does not degrade the conductive element).

Farrar **lacks** the metallic passivating layer 23 being specifically deposited by electroless deposition, i.e., Farrar is silent with respect to the process for depositing the metallic passivating layer 23, which comprises a first barrier layer and a seed layer 26 (e.g., note Col. 5, lines 1-20, wherein Farrar generally recites that "plating layer 23 is deposited..."). Furthermore, note that Farrar is also silent with respect to the process for depositing the first barrier layer or the seed layer. Since Farrar is silent with respect to the deposition process(es), one of ordinary skill in the art would have utilize any suitable process known in the art for depositing the metallic passivating layer 23 (i.e., the seed layer and/or the barrier layer).

Lopatin is **cited to show** it was very well known in the art that an electroless deposition process is well suited for depositing a seed layer (i.e., a metallic passivating layer), which will serve as a catalyst for subsequent plating of a metal layer. Lopatin discloses (in Col. 2, lines 31-37) an electroless deposition process is very well suited for depositing a seed layer over a barrier layer, wherein the seed layer will be utilized in manner that is essentially the same as that described by Farrar (Col. 5, lines 4-6).

Because Farrar does not specify any particular deposition process, which can or cannot be utilized, it would have been obvious to one of ordinary skill in the art to use any well-known, suitable process such as electroless deposition because Lopatin shows that electroless deposition is well suited for forming at least a seed layer, which is very similar to Farrar's seed layer.

Regarding claims 30, 31, 33 and 35:

These claims are essentially drawn to a system for performing the method of claims 24, 26, 28 and/or 29. Since Farrar (in view of Lopatin) discloses all process limitations of the currently claimed invention, it would be readily obvious to one of ordinary skill in the art that Farrar (in view of Lopatin) must incorporate a system comprising means for performing the process steps recited in at least claims 24, 26, 28 and/or 29. Accordingly, these claims are rendered obvious by the cited references.

9. Claims 25 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Farrar** (in view of **Lopatin**) as applied to claims 24 and 30 above, and further in view of Amelio et al. (4,639,380; hereinafter "**Amelio**").

Regarding claim 25:

Farrar (in view of Lopatin) discloses claim 24, and Farrar further discloses depositing the metallic passivating layer comprises the steps of: depositing an initiation layer (i.e., a barrier layer 24, Col. 5, lines 3-4) on the first conductive material 1; and Farrar (in view of Lopatin) discloses depositing a metallic passivating layer on the initiation layer by electroless plating. Farrar (in view of Lopatin) **lacks** exposing the substrate to an activation solution when depositing the initiation layer and specifically disclosing a cleaning step after depositing the initiation layer; however, it is important to note that Farrar does not disclose specific process steps performed during the deposition processes.

Amelio **teaches** it was well known in the art that a substrate must be catalyzed prior to the deposition of metal onto the substrate, and prior to depositing a metallic layer (i.e., a metal

plating) in an electroless plating process, it was also well known to include a cleaning step. Amelio discloses that a typical electroless plating process includes catalyzing a substrate (Col. 1, lines 39-40), wherein the catalyzing process includes depositing an initiation layer by exposing the substrate to an activation solution (e.g., note Col. 3, lines 40-47); cleaning the substrate after forming the initiation/seed layer (Col. 1, lines 58-61); and depositing/plating a metal layer.

Since Farrar (in view of Lopatin) does not provide specific details for depositing the metallic passivating layer, it would have been obvious to one of ordinary skill in the art to form the passivating layer by incorporating a catalyzing and cleaning process as taught by Amelio because the catalyzing and cleaning process would be typically necessary to ensure the quality of the metal coating (i.e., the metallic passivating layer, note Amelio, especially Col. 1, lines 59-61).

Regarding claim 32:

This claim is essentially drawn to a system for performing the method of claim 25. Since Farrar (in view of Lopatin and Amelio) discloses all process limitations of claim 25, it would be readily obvious to one of ordinary skill in the art that Farrar (in view of Lopatin and Amelio) would incorporate a system comprising means for performing the process step recited claim 27. Accordingly, this claim is rendered obvious by the cited references.

10. Claims 27 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Farrar** (in view of **Lopatin**) as applied to claims 24 and 30 above, and further in view of in view of Hashimoto et al. (5,656,128; hereinafter "**Hashimoto**").

Regarding claim 27:

Farrar (in view of Lopatin) **lacks** incorporating an amorphous carbon protective layer. Hashimoto **teaches** that utilizing an amorphous carbon film with a photoresist film improves resolution (i.e., "photolithographic resolution") because the amorphous carbon film serves as an anti-reflective film (note Col. 1, lines 48-59 and Col. 2, lines 7-13). It would have been obvious to one of ordinary skill in the art to modify Farrar (in view of Lopatin) by incorporating an amorphous carbon film as taught by Hashimoto because such a modification could significantly improve "photolithographic resolution". Note that when an amorphous carbon film is incorporated with the photoresist film (in Farrar), the following process steps would result: the amorphous carbon film is deposited over the substrate but underneath the photoresist film, and the amorphous carbon film (and photoresist film) is etched under conditions that do not degrade the conductive element, i.e., the etching is performed to expose the conductive element (as shown in Fig. 8 of Farrar), which is materially different from the photoresist and the amorphous carbon films, accordingly, the conductive element would not be degraded by the etching conditions.

Regarding claim 34:

This claim is essentially drawn to a system for performing the method of claim 27. Since Farrar (in view of Lopatin and Hashimoto) discloses all process limitations of claim 27, it would be readily obvious to one of ordinary skill in the art that Farrar (in view of Lopatin and Hashimoto) would incorporate a system comprising means for performing the process step recited claim 27. Accordingly, this claim is rendered obvious by the cited references.

Remarks

11. Applicant's remarks/arguments have been carefully reviewed and considered, but they are generally not persuasive for the following reasons. With respect to claims 1-5, 7-17, 19-21 and 23, the remarks/arguments are moot in view of the new grounds of rejections. With respect to claims 24-35, it is noted that claim 24 (and claim 30) does not require the substantially flat substrate surface to have/include an "exposed" conductive element, wherein the protective layer is disposed on the substantially flat surface including a surface of the "exposed" conductive film. Furthermore, the examiner disagrees with the applicant's assertion that Farrar fails to teach or suggest a stray metallic passivating material being deposited on the protective layer (see applicant's remarks in the paragraph bridging pages 10-11). As explained above in the rejection of claims 24, 26, 28 and 29, the passivating material 23, which is formed directly on top of layer "21" in Fig. 9 (of Farrar), will be removed when layer "21" is removed; therefore, this portion of the passivation material 23 serves no particular purpose and it can be referred to as a "stray material". Additionally, applicant's assertion, "[t]he use of a blanket deposition layer requires different and less advantageous removal methods...as compared to the stray deposited layer of claims 1, 24 and 30", is not persuasive because Havas and Farrar remove the "blanket-deposited layer" in essentially the same manner as in the current invention, i.e., both Havas and Farrar remove the "blanket-deposited layer" by a "lift-off" process which includes removing the underlying protective/photoresist layer using an etching technique. Therefore, claims 1-5, 7-21 and 23-35 stand rejected under 35 USC § 103.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lex Malsawma whose telephone number is 571-272-1903. The examiner can normally be reached on Mon. - Thur. (4-12 hours between 5:30AM and 10 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lex Malsawma

November 12, 2005

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